A 60 GHz Millimeter-wave MMIC Chipset for Broadband Wireless Access System Front-end

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Abstract — **This paper presents a complete 60 GHz millimeter-wave MMIC chipset for broadband wireless access system. This chipset consists of a low noise amplifier, a power amplifier, an up-converter, a down-converter, a quadrupler and an SPDT switch. Frequency range of these MMICs is from 55 GHz to 64 GHz, this frequency covers the entire 60 GHz application band.**

I. INTRODUCTION

The frequency band of 60 GHz has several advantages for the broadband wireless access system. [1] Data transmission rate up to 1.25Gb/s can be achieved. [2] Atmosphere attenuates RF signals rapidly, making the band ideal for secure transmission over short distances, it can realize reuse of the same frequency without any interference.

Among any components of the 60 GHz broadband wireless system, MMIC is one of the most important elements to decrease the size and cost of the RF front-end module. [3] [4]

In this paper, we present the design, fabrication and performances of the MMICs. All of the MMICs are minimized in chip-size by using 28-μm-thick substrate. [5] Using these MMICs, a complete front-end for broadband wireless access can be easily designed in a short period.

II. CHIPSET DESCRIPTION

An example of the 60 GHz broadband wireless access front-end block diagram is shown in Fig.1.

This front-end is composed of low noise amplifiers (LNA), a power amplifier (PA), an up-converter, a down-converter, a quadrupler and two single pole double throw (SPDT) switches.

In our design, all of the MMICs consists of InGaP/InGaAs pseudomorphic HEMT (p-HEMT), which are fabricated on a 4-inch semi-insulated GaAs substrate with a 0.15-μm-long T-shaped gate electrode. This process technology is the same as our millimeter-wave MMIC process. [5] For the SPDT switch and the down-converter, p-HEMTs are used as Schottky diodes for wide band operation. Substrate thickness of the MMIC is thinned to 28 μm by using mechanical and chemical etching. By using the thin substrate, microstrip-line-width, line to line space and via hole area can be reduced and that die size of the MMIC becomes small.

In this design, we considered parasitic inductance of bonding wires. All of the measurement data includes the bonding wire inductance.

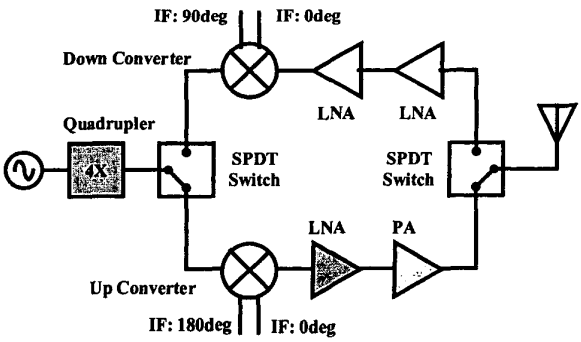

Fig. 1. An example of the 60 GHz broadband wireless accesses system front-end block diagram.

III. MMIC DESIGN AND PERFORMANCES

A. Low Noise Amplifier (LNA)

A photograph and a schematic of the LNA are shown in Fig.2. The LNA is designed as a three-stage single-ended amplifier. To decrease the die-size, gate-width of the first and the second stage is optimized for minimizing matching circuit. The gate-width of the first and the second stage is 80 μm and third-stage is 160 μm. The die-size of the LNA is 0.9 mm^2. Figure 3 gives a characteristic of noise figure

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and gain. Noise figure is less than 5 dB, gain is more than 18.5 dB from 55 GHz to 65 GHz. The saturated output power of the LNA is 9dBm.

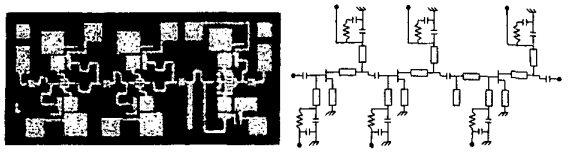

Fig. 2. Photograph and schematic of the LNA
Chip dimensions: 1.33 x 0.68 mm

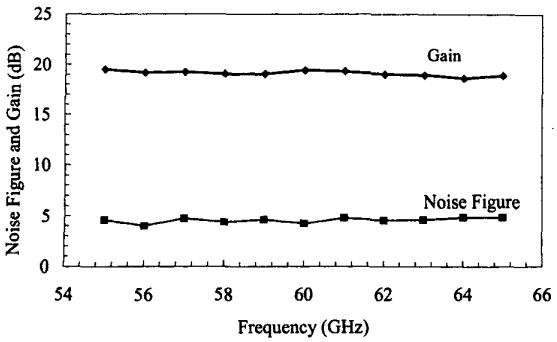

Fig. 3. Measured noise figure and gain of the LNA
VDD = 3V, VGG = -0.1V, IDD = 21 mA

B. Power Amplifier (PA)

The power amplifier is designed as a three-stage amplifier employing four 320-μm gate-width p-HEMTs. The first and the second stages are single-ended amplifiers, a Wilkinson divider and a combiner are used as matching circuit for third-stage of the power amplifier to flatten frequency response. The circuit schematic of the power amplifier is shown in Fig.4.

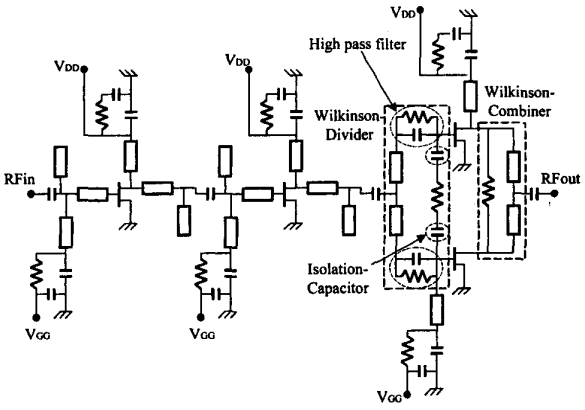

Fig. 4. Schematic diagram of the power amplifier

To prevent lower frequency oscillation, high-pass filters are placed at the input ports of the third stage p-HEMTs. Two capacitors are connected to an isolation-resistor of the Wilkinson divider in series connection, these capacitors compensate parasitic inductance between the divider output ports, and enhance isolation of the divider. The photograph of the power amplifier is shown in Fig.5.

Measured result of the output power is shown in Fig.6. The output power is more than 14 dBm at 3-dBm input power, the small signal gain is more than 15 dB from 55 GHz to 64 GHz. [6]

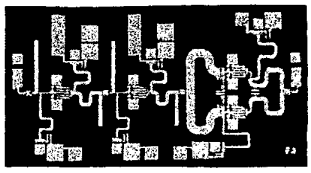

Fig. 5. Photograph of the power amplifier
Dimensions: 1.98 x 1.1 mm

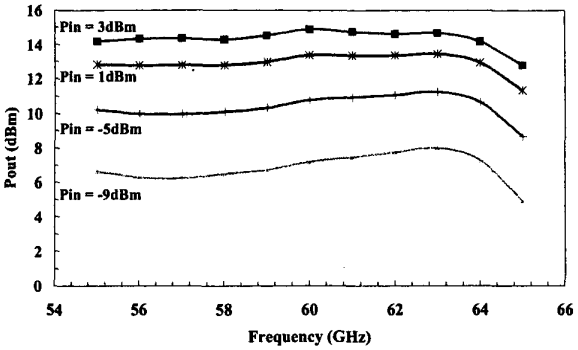

Fig. 6. Measured output power of the power amplifier
VDD = 3V, VGG = 0V, IDD = 160 mA @ Pin = -9dBm

C. Up-Converter

The circuit of an up-converter is LO suppression mixer. Figure 7 shows the photograph and the schematic of the up-converter, consisting of two 90°-hybrid-couplers and two p-HEMTs. These p-HEMTs are operated below threshold voltage.

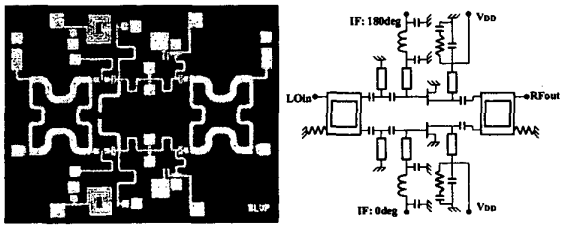

Fig. 7. Photograph and schematic of the up-converter
Dimensions: 1.67 x 1.34 mm

Figure 8 shows the measured results of an up-converter. The measured conversion loss is about 15 dB from 50 GHz to 70 GHz, local power suppression, compared to the input local signal level, is more than 15 dBc.

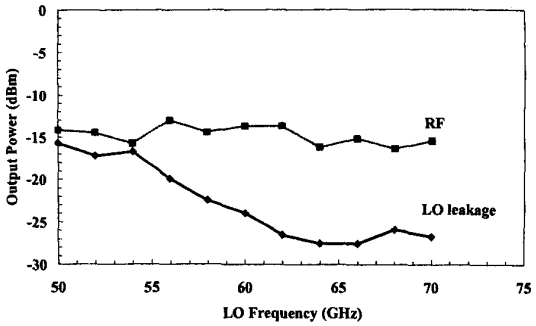

Fig. 8. Measured results of the up-converter
V_{DD} = 3V, V_{GG} = -0.3V, Plo = 0 dBm, Pif = 0 dBm
Fif = 2 GHz, Frf > Flo

D. Down-Converter

The down-converter is designed as an image rejection mixer. Figure 9 shows the photograph of the down-converter, consisting of a 90°-hybrid-coupler, a Wilkinson coupler and two p-HEMTs that are used as Schottky diodes. No external DC bias is required.

Figure 10 shows the conversion gain and the image rejection ratio. The conversion gain is more than -15 dB, the image rejection ratio, compared to the RF signal level, is better than 20 dBc from 54 GHz to 64 GHz. [7]

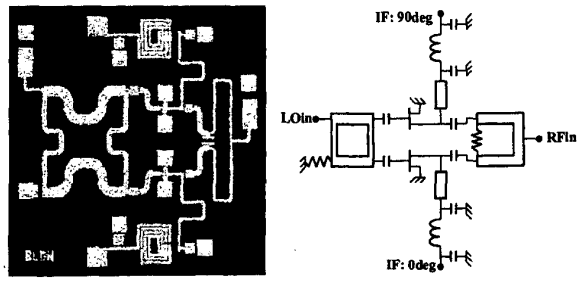

Fig. 9. Photograph and schematic of the Down-converter
Dimensions: 1.18 x 1.2 mm

E. Quadrupler

The quadrupler MMIC is composed of an active balanced quadrupler and a three-stage buffer amplifier, as shown in Fig.11.

The quadrupler element is a parallel connection of a common-gate and a common-source p-HEMT. Odd-harmonics are suppressed by the difference of S21 phase each p-HEMT. [8] The second harmonic is suppressed by frequency response of the three-stage amplifier. The photograph of the quadrupler is shown in Fig.12.

Figure 13 shows the output power of the fourth harmonic signal and undesired harmonics signals. The output power of the fourth harmonic signal is more than 3dBm from 55 GHz to 64 GHz at 10 dBm input power level.

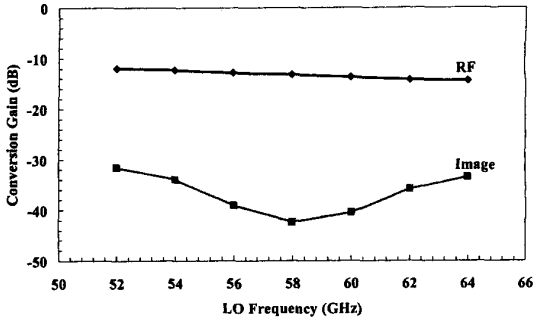

Fig. 10. Measured results of the down-converter
Plo = 0 dBm, Prf = -20 dBm, Fif = 2 GHz, Frf > Flo

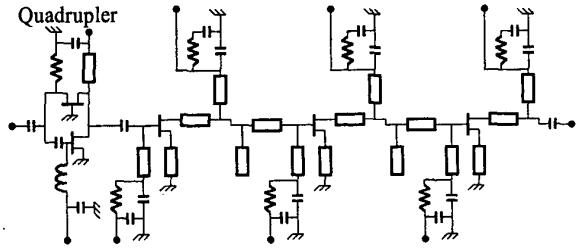

Fig. 11. Schematic diagram of the quarupler

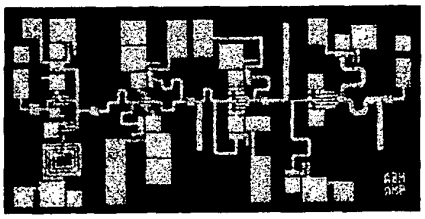

Fig. 12. Photograph of the quadrupler
Dimensions: 1.86 x 0.96 mm

F. SPDT Switch

The SPDT switch design is based on our previous work. [9] The switch design utilizes distributed 5-shunt diodes. By using 28-μm-thick substrate, the chip area was reduce to 1/4 compared to the design was done by using 75-μm thick-substrate. Figure 14 shows the photograph of the SPDT switch.

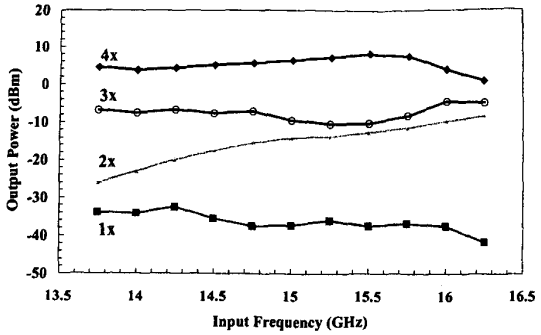

Fig. 13. Measured results of the quadrupler
VDMLT, VDAMP, = 3V, VGMLT = -0.5V, VGAMP = 0V
Pin = 10 dBm

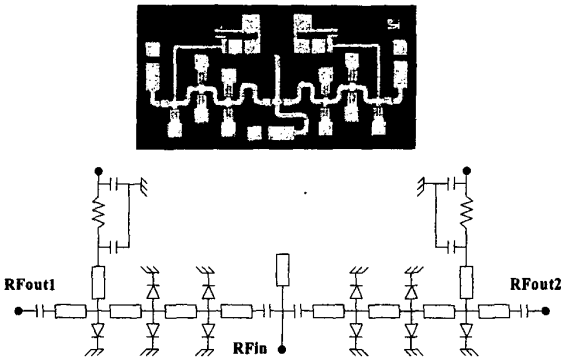

Fig. 14. Photograph and schematic of the SPDT switch
Dimensions: 1.36 x 0.75 mm

Figure 15 shows the small signal performances of the insertion loss at the ON-state and the isolation at the OFF-state. One unused port was terminated with a 50-ohm load. The insertion loss is less than 2.5 dB and the isolation is greater than 35 dB from 55 GHz to 70 GHz.

V. CONCLUSION

This paper describes the design, fabrication and performances of the 60 GHz MMIC chipset for the front-end of the broadband wireless access system. We have successfully developed complete MMIC chipset that are LNA, power amplifier, up-converter, down-converter, and quadrupler, SPDT switch.

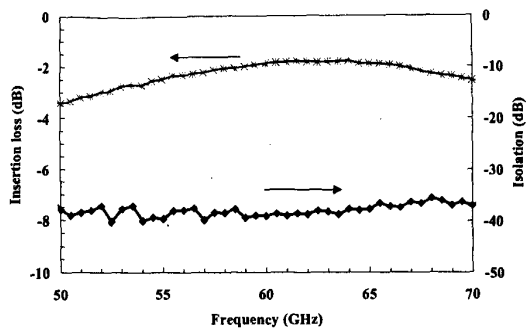

Fig. 15. Measured results of the SPDT switch
VDD = -2V, + 2V

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